Section I. (Amendments to the Claims)

Following is a listing of claims 1-20 as amended herein, with markings to show changes made:

1-12. (Cancelled).

13. (Currently amended) A ~~thin film insulating (FIN)~~ double-gated/double-channel FIN metal oxide semiconductor field effect transistor (MOSFET) comprising:

a bottom Si-containing layer;

an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein;

a gate region in said partial opening, said gate region comprising two regions of gate conductor that are separated from vertical fin-shaped silicon-containing channel regions by an insulating film, said insulating film comprising a gate dielectric and having opposite vertical surfaces adjacent to the vertical fin-shaped silicon-containing channel regions;

source/drain diffusion regions abutting said gate region, said source/drain diffusion regions having junctions that are self-aligned to the vertical fin-shaped silicon-containing channel regions and the gate region; and

insulating spacers in said partial opening that separate the gate region and the source/drain diffusion regions formed orthogonal to said insulating film; ~~and~~

wherein said gate region is between said insulating spacers; and

wherein ~~said MOSFET is a double-gated/double-channel MOSFET device, in which~~ the gate region is self-aligned to the source/drain diffusion regions and the vertical fin-shaped silicon-containing channel regions.

14. (Original) The FIN MOSFET of Claim 13 wherein said insulating region includes an insulating layer of an SOI material.

15. (Currently amended) The FIN MOSFET of Claim ~~13~~ 14 wherein said partial opening exposes a portion of said insulating layer of said SOI material.

16. (Previously presented) The FIN MOSFET of Claim 13 wherein said insulating film is formed surrounding a portion of a Si-containing layer.

17. (Currently amended) The FIN MOSFET of Claim 16 wherein ~~said~~ the gate dielectric of said insulating film is comprises of an oxide, a nitride, an oxynitride or any combination or multilayer thereof.

18. (Original) The FIN MOSFET of Claim 13 wherein said regions of gate conductor are each comprised of polysilicon, amorphous Si, a conductive elemental metal, an alloy of a conductive elemental metal, a nitride or silicide of a conductive elemental metal or multilayers thereof.

19. (Original) The FIN MOSFET of Claim 13 further comprising salicide regions formed atop said source/drain diffusion regions.

20. (Original) The FIN MOSFET of Claim 13 wherein said source/drain diffusion regions are formed in a portion of a patterned Si-containing layer.